

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

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U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HAO FANG, YUE-SONG HE, MARK S. CHANG
and KENT K. CHANG

Appeal No. 2005-0316
Application No. 09/941,370¹

ON BRIEF

Before GROSS, BARRY and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1, 2 and 10. Claims 5-9, 11 and 12 have been canceled and claims 3 and 4 have been indicated by the Examiner as being allowable.

We affirm-in-part.

BACKGROUND

Appellants' invention is directed to enhancing the gate oxide in the core area of memory devices using a nitridation

¹ Application for patent filed August 28, 2001 which according to Appellants, is a divisional of application No. 09/595,422, filed June 15, 2000, now abandoned.

process without affecting the quality of the gate oxide in the periphery areas. According to Appellants, a nitridation process to improve the reliability of the core gate oxide is problematic for the peripheral devices since the presence of nitrogen residue in the silicon interface inhibits the subsequent growth of oxide in those areas (specification, page 2). Appellants' invention includes processing steps for providing a portion of a dual gate oxide in the periphery area and then simultaneously providing a dual gate oxide in a core area and completing the dual gate oxide in the periphery area of the memory before the nitridation step (specification, page 3). An understanding of the invention can be derived from a reading of exemplary independent claim 1, which is reproduced as follows:

1. A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate; and

(c) strengthening the interface by providing a nitridation process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area.

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The Examiner relies on the following references:

Holler et al. (Holler)	4,780,424	Oct. 25, 1988
Lee	5,175,120	Dec. 29, 1992
Cappelletti et al. (Cappelletti)	5,637,520	Jun. 10, 1997
Wristers et al. (Wristers)	5,674,788	Oct. 7, 1997
Takebuchi	6,417,051	Jul. 9, 2002 (filed March 10, 2000)

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Cappelletti combined with Takebuchi, Holler or Wristers.

Claims 2 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cappelletti combined with Takebuchi, Holler or Wristers and further in view of Lee.

Rather than reiterate the opposing arguments, reference is made to the briefs and answer for the respective positions of Appellants and the Examiner. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the brief have not been considered (37 CFR § 41.67(c)(1)(vii)).

OPINION

As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting

a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In order to establish a prima facie case of obviousness, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). However, the motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

With respect to claim 1, Appellants argue that since each applied reference is directed to a different memory device, one of ordinary skill in the art would not be motivated to combine their teachings (brief, pages 3-5). Appellants further assert differences in the principle of operation in each reference and argue that the combination of Cappelletti with other applied

prior art would render the results inoperable (brief, pages 5-11). The Examiner responds by pointing to teachings in each of Takebuchi, Holler and Wristers regarding the desirability of the nitridation process for improving the quality of the gate oxides (answer, page 5).

Upon a review of the references, we disagree with Appellants that the benefits of nitridation process cannot be obtained by the combination because the method of gate oxide processing disclosed in each applied prior art is used in a different memory device. Takebuchi, Holler and Wristers are all concerned with improved reliability of the gate oxide by providing a nitridation process after the gate oxide layer is formed. In fact, process steps are like the steps of a recipe that may be adjusted and modified to make different devices. In that regard, we note that the kind of memory device is not relevant as long as the disclosed enhancements to the process steps are used to improve elements such as the gate oxide, which are common to different devices formed according to such process steps.

Additionally, contrary to Appellants' view (reply brief, page 5) and as argued by the Examiner (answer, page 7), the combination is not based on bodily incorporation of the disclosed features of Takebuchi, Holler or Wristers in Cappelletti, but on

what the reference teachings would have suggested to the skilled artisan. In other words, all of the features of the secondary reference need not be bodily incorporated into the primary reference (see In re Keller, 642 F.2d at 425, 208 USPQ at 881 (CCPA 1981)) and the artisan is not compelled to blindly follow the teaching of one prior art reference over the other without the exercise of independent judgment (see Lear Siegler, Inc. v. Aeroquip Corp., 733 F.2d 881, 889, 221 USPQ 1025, 1032 (Fed. Cir. 1984)). In fact, to the extent that there is no per se rule for designating a reference primary or secondary and how its teachings may be stacked up with the others, we find that the Examiner has reasonably started with Cappelletti as it discloses most of the claimed steps for forming the core and periphery gate oxides.

Furthermore, we remain unpersuaded by Appellants' argument that the references teach away from the combination (brief, pages 5-11; reply brief, page 8) and find that introducing nitrogen in the tunnel gate oxide in the core area is actually suggested by each of the applied references. While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the

combination (see B.F. Goodrich Co. v. Aircraft Braking Systems Corp., 72 F.3d 1577, 1583, 37 USPQ2d 1314, 1319 (Fed. Cir. 1996) and In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988)) as the appellants would apparently have us believe. We also note that the motivation to combine prior art references may be found in the nature of the problem to be solved. Ruiz v. A.B. Chance Co., 357 F.3d 1270, 1276, 69 USPQ2d 1686,1690 (Fed. Cir. 2004). As argued by the Examiner (answer, page 5) and shown above, Takebuchi, Holler and Wristers are concerned with improving the gate oxide quality and suggest the desirability of using nitridation process. Therefore, the teachings of Takebuchi, Holler and Wristers are relevant to Cappelletti and their combination would have been obvious to one of ordinary skill in the art.

Appellants further argue that the combination of the references fails to teach the claimed step of nitridation both after providing a portion of the periphery gate oxide and after simultaneously providing the core gate oxide and completing the periphery gate oxide (brief, page 12). Although the Examiner addresses this argument as a part of the stated rejection (brief, page 4), it is reasonably clear that the Examiner proposes adding the nitridation process after the gate oxide in the core area is

formed which is after forming the oxides in both the core and periphery areas.

Cappelletti discloses a process for fabricating the transistors both in the cell or core area and in the transistor or periphery area using a double poly process (col. 2, lines 13-22). As depicted in Figures 10 and 11, a portion of dual gate oxide layer 35' in periphery area 32 is grown and masked while oxide 35 in core area 31 is removed (col. 4, lines 20-36). Next, after removing the mask layer covering oxide 35', dual gate oxide layer 61 in core area 31 is grown through an oxidation process which also increases the thickness of gate oxide layer 35" in the periphery area while completing the formation of that oxide (Figure 12; col. 4, lines 36-48). After completing the gate oxide layer in both the core and the periphery areas, gate poly layers are deposited (col. 4, lines 49-67).

Takebuchi, on the other hand, relates to using a nitridation process for the tunnel insulating layer in the memory cell or the core area for improving the storing capability of the memory element (abstract; col. 1, lines 45-48). However, as the nitridation process may adversely affect the performance of the transistors in the periphery area, Takebuchi suggests lowering the nitrogen density in the gate oxide in the periphery area

through protecting the periphery area during the nitridation process of the tunnel oxide layer in the cell or the core area, (abstract; col. 3, lines 23-28). The approach Takebuchi takes, as depicted in Figures 4(A)-4(E), includes forming the tunnel oxide layer first and therefore, requires limiting nitridation to the core areas by using buffer oxide layer 65 in the periphery area while nitrogen is added to gate oxide 61 in the core area (col. 12,, lines 4-32).

Similarly, Holler suggests enhancing the gate oxide quality by nitridation of the gate oxide in the memory cell or the core area (col. 5, lines 6-15). Wristers also discloses the advantages of introducing nitrogen into the gate oxide of MOS transistors (abstract; col. 3, lines 40-43). Thus, having each of these references available, one of ordinary skill in the art would have found it obvious to improve the gate oxide quality by introducing nitrogen into the gate oxide layer in the core area of a memory element.

In this case, although the nitridation process is adapted to the specific process sequence employed in each of Takebuchi, Holler and Wristers, they all require that nitrogen be introduced after the tunnel gate oxide in the core area is formed. Modifying Cappelletti as such would require adding nitrogen to

gate oxide layer 61 after its formation (Figure 12) and before the gate electrode 41 is deposited (Figure 13). Therefore, performing the nitridation process in Cappelletti after providing the gate oxide in the core area would also take place after both providing a portion of the periphery gate oxide as layer 35' and later completing it as layer 35" simultaneous with the formation of core gate oxide 61, as required by claim 1.

In view of the analysis above, we find the Examiner's reliance on the combination of Cappelletti with each of Takebuchi, Holler or Wristers to be reasonable and sufficient to support a prima facie case of obviousness. Accordingly, we sustain the 35 U.S.C. § 103 rejection of independent claim 1.

With respect to claims 2 and 10, Appellants argue that the combination of Lee with the references applied to the base claim fails to show how the layer of oxide nitride and a portion of the layer of type-1 polysilicon layer are removed from the periphery area (brief, page 15; reply brief, page 10). We agree with Appellants and note that Lee removes the entire polysilicon layer from the periphery area (col. 3, lines 26-28) instead of "a portion of the layer of type-1 polysilicon," as required by the claims. Accordingly, the 35 U.S.C. § 103 rejection of claims 2 and 10 cannot be sustained.

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CONCLUSION

In view of the foregoing the decision of the Examiner rejecting claim 1 under 35 U.S.C. § 103 is affirmed but is reversed with respect to claims 2 and 10.


No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

Anita Pellman Gross
ANITA PELLMAN GROSS
Administrative Patent Judge

~~LANCE LEONARD BARRY~~
~~Administrative Patent Judge~~

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